
Contents

<i>Preface</i>	<i>vii</i>
1. Logic Gates	1
1.1 Introduction	1
1.2 The Inverter (NOT Gate)	2
1.3 The AND Gate	3
1.4 The OR Gate	5
1.5 The NAND Gate	6
1.6 The NOR Gate	7
1.7 The Exclusive-OR Gate	8
1.8 The Exclusive-NOR Gate	8
1.9 Digital Integrated Circuits	9
1.10 Digital IC Logic Families	9
Solved Problems	11
Exercises	13
2. Boolean Algebra	14
2.1 Logic Expressions	15
2.2 Laws, Postulates and Theorems	16
2.3 De Morgan's Theorems	17
2.4 Boolean Functions	18
Complement of a Function	19
2.5 Canonical Forms	20
Minterm Canonical Form (Sum of Minterms)	21
Maxterm Canonical Form (Product of Maxterms)	21
Conversion between Canonical Forms	22
Conversion of a Truth Table to Canonical Forms	23

2.6	Standard Forms	24
	Solved Problems	24
	Exercises	31
3.	Simplification of Boolean Functions	34
3.1	The K-map Method	34
	Plotting a K-map	36
	Grouping	38
	Rules	38
	Simplification	38
3.2	SOP and POS Simplification	40
3.3	Don't Care Conditions	41
3.4	NAND and NOR Implementation	42
3.5	Quine-McCluskey Method (The Tabulation Method)	45
3.6	Determination of Prime-implicants	46
3.7	Selection of Prime-implicants	48
3.8	Quine-McCluskey Method for 'Don't Care' Problems	50
3.9	Comparison of K-map and Quine-McCluskey Methods	52
	Solved Problems	52
	Exercises	66
4.	Combinational Logic	67
4.1	Design Procedure	67
4.2	Adders and Subtractors	68
	Half-Adder	68
	Full-Adder	70
	Half-Subtractor	73
	Full-Subtractor	75
4.3	Code Converters	78
4.4	Analysis Procedure	81
4.5	Multilevel NAND Circuits	84
4.6	Multilevel NOR Circuits	88
4.7	Exclusive-OR and Equivalence (i.e. Ex-NOR) Functions	89
4.8	Parity Generator and Checker	91
	Solved Problems	93
	Exercises	101
5.	Combinational Logic with MSI and LSI	103
5.1	Binary Parallel Adder	103
	The Ripple-Carry Adder	104
	The Look-Ahead-Carry Adder	105
	The 74S182 Look-Ahead Carry Generator	107
	The 74283 4-Bit Binary Parallel Adder	110
5.2	BCD Adder	112

5.3	Magnitude Comparator	114
	The 7485 Magnitude Comparator	116
5.4	Decoders	118
	The 74LS138 3-Line to 8-Line Decoder	119
	The 7442 4-line BCD to 10-Line Decimal Decoder	121
	Combinational Logic Using Decoders	124
5.5	Encoders	124
	The Priority Encoder	125
	The 74148 8-Line to 3-Line Priority Encoder	126
5.6	Multiplexers (Data Selectors)	128
	The 74157 Quadruple 2-Line to 1-Line Multiplexer	129
	Implementation of Boolean Function Using Multiplexers	132
5.7	Demultiplexers (Data Distributors)	133
	Solved Problems	134
	Exercises	144
6.	Sequential Logic	146
6.1	Flip-Flops	147
6.2	Latches	147
	The NOR Gate <i>S-R</i> Latch	147
	The NAND Gate <i>S-R</i> Latch	149
6.3	Clock Signals and Clocked-Mode Flip-Flops	150
	Clock Signals	150
	Clocked-Mode Flip-Flops	150
	Setup Time and Hold Time	151
	Edge-Triggered <i>S-R</i> Flip-Flop	151
	Edge-Triggered <i>D</i> Flip-Flop	153
	Edge-Triggered <i>J-K</i> Flip-Flop	154
	Edge-Triggered <i>T</i> Flip-Flop	156
	<i>J-K</i> Master-Slave Flip-Flop	157
	Asynchronous Inputs	159
6.4	Counters	159
6.5	Asynchronous (Ripple) Counters	161
	3-Bit Asynchronous Binary Up-Counter	161
	Counter as a Frequency Divider	162
6.6	Asynchronous Counters with MOD Numbers $<2^n$	162
	Design Procedure to Construct Asynchronous (Ripple) Counters	164
6.7	Propagation Delay in Ripple Counters	164
6.8	IC Asynchronous Counters	164
	The 7490 Decade Counter	164
	The 7493 4-Bit Binary Ripple Counter	166
6.9	Asynchronous Down Counter	168
	3-Bit Asynchronous Binary Down-Counter	168
6.10	Analysis of Clocked Sequential Circuits	170
	State Table	170

Derivation of the State Table	170
State Diagram	171
6.11 Flip-Flop Excitation Tables	172
6.12 Synchronous (Parallel) Counters	173
Synchronous Counter Design by Inspection	174
6.13 Synchronous Down and Up/Down Counters	175
6.14 Presettable Counters	176
The 74193 Presettable 4-Bit Binary Up/Down Counter	177
6.15 Synchronous Counter Design by Systematic Procedure	179
6.16 Shift Registers	183
Serial In-Serial Out (SISO) Shift Registers	185
Serial In-Parallel Out (SIPO) Shift Registers	186
Parallel In-Serial Out (PISO) Shift Registers	186
Parallel In-Parallel Out (PIPO) Shift Registers	187
6.17 Bidirectional Shift Registers	188
The 74194 4-Bit Bidirectional Universal Shift Register	188
6.18 Shift Register Counters	190
The Ring Counter	190
The Johnson Counter	191
6.19 Schmitt-Trigger Devices	192
6.20 One-Shot (Monostable Multivibrator)	193
Nonretriggerable One-Shot	194
Retriggerable One-Shot	194
6.21 Clock Generator Circuits	195
Clock Circuit Using Schmitt-Trigger INVERTER	195
Clock Circuit Using the 555 Timer	195
Solved Problems	196
Exercises	209
7. Memory Devices	211
7.1 Memory Terminology	212
7.2 General Memory Operation	213
7.3 CPU-Memory Connections	214
7.4 Read-Only Memories (ROMs)	215
ROM Architecture	215
7.5 Types of ROMs	216
Masked ROM (MROM)	216
Programmable ROM (PROM)	218
Erasable Programmable ROM (EPROM)	218
Electrically Erasable PROM (EEPROM)	218
Flash Memory	218
7.6 Applications of ROM	218
7.7 Programmable Logic Devices (PLDs)	219
PLD Symbolology	220
7.8 Programmable Array Logic (PAL)	221

7.9 Programmable Logic Array (PLA)	223
7.10 Read/Write Random Access Memories (RAMs)	223
RAM Architecture	224
7.11 Static Ram (SRAM)	225
Read Cycle	225
Write Cycle	226
7.12 Dynamic Ram (DRAM)	227
DRAM Structure and Operation	228
Read Cycle	229
Write Cycle	230
7.13 Expanding Word Size and Capacity	231
Expanding Word Size	231
Expanding Word Capacity	232
7.14 Special Memory Functions	233
Solved Problems	234
Exercises	238
<i>Answers to Exercises</i>	240
<i>References</i>	247
<i>Appendix – Digital ICs</i>	249
<i>Index</i>	255